

Mimosa_5 Programs with scope trigger:

Scope trigger set for delay that puts trigger at first pixel of each frame

512rg4m4d522p0x512x512.mcs

512rg4m4d522p512x512.mcs

512rg4m4d522p2x512x512.mcs

512rg4m4d522p3x512x512.mcs

test pin outs:

FPGA File:	512rg4m4d522 xxxxx .mcs		
J11 test point numbering J11-25 = tpb1 J11-23 = tpb2		FPGA pins	Connection
tpb1 25	debugA	R18	clk_acq
tpb2 23	debugB	R19	acq_finished (toggles)
tpb3 21	debugC	R20	trg_out (added adjustable scope trg)
tpb4 19	debugD	R21	chp_rstdb (same as chp_rst)
tpb5 17	debugE	R22	rowmk0 (marker from chip)
tpb6 15	debugF	P19	acq_active
tpb7 13		P20	
tpb8 11		P21	
tpb9 9		P22	section<0> select section with two bits
tpb10 7		P18	section<1>
tpb11 5		N18	grd to kill acq_en ?
tpb12 3		N19	grd to kill row marker ?

Selecting the quadrant for data storage:

Quadrant		J11-7 bit	J11-9 bit
Top Right	VREFTR	0	0
Bottom Right	VREFBR	0	1
Top Left	VREFTL	1	0
Bottom Left	VREFBL	1	1